**Title:**

Design and Verification of an ATM Machine Controller with Verilog.

**Abstract:**

This Verilog code provides an extended simulation of an Automated Teller Machine (ATM) with added features. The design has evolved to encompass various functions like cash withdrawal, depositing money, checking account balance, changing the PIN, and handling other inquiries. Utilizing a finite state machine (FSM) structure, the code guides the ATM through different states to manage diverse user interactions. Despite its simplicity, this model aims to serve as a flexible foundation for more advanced ATM systems. It emphasizes modularity, enabling further enhancements and considerations for real-world security measures. This expanded version aims to offer a more comprehensive representation of an ATM in Verilog, demonstrating its adaptability for broader applications.

**Outcomes:**

1. The project provides a functional simulation of an ATM system, allowing users to interact with features such as withdrawal, deposit, balance inquiry, PIN change, and other inquiries.
2. The code implements a Finite State Machine (FSM) architecture, aiding in understanding how to manage different states and transitions within the ATM system.
3. While the code remains simple, it provides a foundation that can be built upon for more realistic and secure ATM system implementations. Real-world considerations, such as security measures and user authentication, can be incorporated based on project requirements.
4. The Verilog code follows coding practices such as state-based design, sequential logic, and conditional statements, providing a practical example for learners and developers.